**COEN 210 Project #2, Spring 2018**

In this project, we have modeled a 4 pipeline stages RISC-V microprocessor in C++ with the given 2 trace files.

Three experiments were conducted and the result with observation is listed below:

Experiment 1 : On original experiment.

Experiment 2 : On doubling the miss rate for instruction cache and same data cache miss rate.

Experiment 3 : On halving the miss rate of data cache and same instruction cache miss rate as in original case.

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| --- | --- | --- | --- |
| **Statistical Data** | **Experiment 1** | **Experiment 2** | **Experiment 3** |
| Num\_data\_cache\_load\_acc | 25531 | 25531 | 25531 |
| Num\_data\_cache\_store\_acc | 23052 | 23052 | 23052 |
| Num\_instr\_cache\_acc | 123657 | 123657 | 123657 |
| Num\_instr\_cache\_hits | 122657 | 120660 | 123654 |
| Num\_data\_cache\_hits | 22530 | 22031 | 24029 |
| Num\_alu\_instr | 53060 | 53060 | 53060 |
| Num\_branch\_instr | 22014 | 22014 | 22014 |
| Num\_load\_instr | 25531 | 25531 | 25531 |
| Num\_store\_instr | 23052 | 23052 | 23052 |
| Num\_all\_other\_instr | 0 | 0 | 0 |
| Num\_taken\_branches | 15013 | 15013 | 15013 |
| Num\_fwd\_from\_EX\_stage | 18508 | 18509 | 20007 |
| Num\_fwd\_from\_MEM\_stage | 18517 | 18017 | 19016 |
| Num\_cycles\_stalled\_in\_ID\_stage | 36993 | 40985 | 19007 |
| Total\_num\_of\_cycles | 192164 | 224114 | 160220 |
| **Calculation:** | **Experiment 1** | **Experiment 2** | **Experiment 3** |
| Instruction Hit Ratio: | 0.99191 | 0.97576 | 0.99998 |
| Data Cache Hit Ratio: | 0.88246 | 0.86291 | 0.94117 |
| Instruction per Clock Cycle: | 0.6435 | 0.55176 | 0.7718 |
| Percentage of taken branches over total branches: | 0.68198 | 0.68198 | 0.68198 |
| Instruction type frequency for ALU: | 0.42909 | 0.42909 | 0.42909 |
| Instruction type frequency for load: | 0.20647 | 0.20647 | 0.20647 |
| Instruction type frequency for store: | 0.18642 | 0.18642 | 0.18642 |
| Instruction type frequency for branch: | 0.17802 | 0.17802 | 0.17802 |
| Percentage of stalled cycles over total cycles: | 0.19251 | 0.18288 | 0.11863 |

**Observation:**

1. Instruction type frequency for ALU, load, store and branch remain the same for all three experiments.
2. Percentage of stalled cycles over total cycles:

* On doubling the miss rate for instruction cache and same data cache miss rate, it is decreased from the original scenario.
* On halving the miss rate of data cache and same instruction cache miss rate as in original case, it is decreased further.

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2. Instruction per Clock Cycle:

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